DETAILED ACTION

Examiner's Amendment

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Mr John Sensny on July 02, 2012.

Please amend claims 1, 3, 7, 13 and 16 - 17 filed June 11, 2012, as follows:

1. A method of synchronizing the frequency of a local clock of a digital data decoder with the frequency of a program clock, wherein the decoder includes clock adjustment hardware for adjusting the local clock frequency and a processing unit for executing software programs and having a clock adjustment software program for adjusting the local clock frequency, the method comprising the steps of:

determining the difference between the local and program clock frequencies, then adjusting the frequency at which the local clock oscillates so that said difference approaches zero, including the steps of:

using the clock adjustment hardware to adjust the local clock frequency until a threshold condition occurs[,]; and

after the threshold condition occurs, using the software program executing on the processing unit to adjust the local clock frequency[.];

<u>wherein the adjusting the frequency at which the local clock oscillates includes switching between using said clock adjustment hardware and using said clock adjustment software program executing on the processing unit to adjust the frequency at which the local clock oscillates.</u>

3. A method of synchronizing the frequency of a local clock of a digital data decoder with the frequency of a program clock, wherein the local clock oscillates at a local clock frequency, the method comprising the steps of:

determining the difference between the local and program clock frequencies, then adjusting the frequency at which the local clock oscillates so that said difference approaches zero;

maintaining a local clock value based on the oscillations of the local clock;

receiving program clock data at the decoder which specify the program clock frequency;

maintaining a program clock value based on the program clock data received at the decoder;

determining if there is an absolute difference between the local clock value and the program clock value;

if there is an absolute difference between the local clock value and the program clock value, then adjusting the frequency at which the local clock oscillates so that said absolute difference approaches zero;

wherein the decoder includes clock adjustment hardware for adjusting the local clock frequency and a processing unit for executing software programs and having a clock adjustment software program for adjusting the local clock frequency, and wherein the step of adjusting the frequency of the local clock includes the steps of:

using the clock adjustment hardware to adjust the local clock frequency until a threshold condition occurs; and

after the threshold condition occurs, using the software program executing on the processing unit to adjust the local clock frequency[.];

wherein the adjusting the frequency at which the local clock oscillates includes switching between using said clock adjustment hardware and using said clock adjustment software program executing on the processing unit to adjust the frequency at which the local clock oscillates.

7. A system for adjusting a local clock on a digital data decoder, wherein the clock oscillates at a local clock frequency, the system comprising:

a system time clock register for maintaining a local clock value based on the oscillations of the local clock;

means for receiving program clock data transmitted to the decoder that specify a program clock frequency;

a program clock register for maintaining a program clock value based on the clock data transmitted to the decoder;

means for determining if there is any difference between the local clock and the program clock frequencies;

a transport demultiplexer for determining if there is an absolute difference between the local clock value and the program clock value; and

means for adjusting the frequency at which the local clock oscillates, when there is a difference between the local clock and the program clock frequencies or an absolute difference between the local clock value and the program clock value, so that said difference approaches zero;

wherein the means for adjusting the frequency at which the local clock oscillates includes:

clock adjustment hardware for adjusting the local clock frequency until a threshold condition occurs; and

a processing unit for executing software programs ~~and having~~ and configured for executing a clock adjustment software program for adjusting the local clock frequency after the threshold condition occurs[.];

<u>wherein the means for adjusting the frequency at which the local clock oscillates further includes switching between using said clock adjustment hardware and using said clock adjustment software program executing on the processing unit to adjust the frequency at which the local clock oscillates.</u>

13. A system for synchronizing the frequency of a local clock of a digital data decoder with the frequency of a program clock, comprising:

means for determining if there is any difference between the local and program clock frequencies; and

means for adjusting the frequency at which the local clock oscillates, when there is a difference between the local clock and the program clock frequencies, so that said difference approaches zero, wherein the means for adjusting includes:

i) clock adjustment hardware on the decoder for adjusting the local clock frequency until a threshold condition occurs, and

ii) a processing unit for executing software programs ~~and~~ on the decoder ~~and having~~ and configured for executing a clock adjustment software program for adjusting the local clock frequency after the threshold condition occurs[.];

wherein the means for adjusting the frequency at which the local clock oscillates further includes switching between using said clock adjustment hardware and using said clock adjustment software program executing on the processing unit to adjust the frequency at which the local clock oscillates.

16. (Cancelled)

17. The method according to Claim [16] 1, wherein:

the threshold condition is an adjustable value; and

the switching between using said clock adjustment hardware and using said clock adjustment software program includes:

setting a first value for the threshold condition;

switching from using the clock adjustment hardware to using the clock adjustment software to adjust the frequency at which the local clock oscillates when the difference between the frequencies of the local clock and the program clock is greater than said first value;

after switching from using the clock adjustment hardware to using the clock adjustment software to adjust the frequency at which the local clock oscillates, setting a second value for the threshold condition, said second value being less than said first value; and

switching from using the clock adjustment software to using the clock adjustment hardware to adjust the frequency at which the local clock oscillates when the difference between the frequencies of the local clock and the program clock falls below said second value.

Allowable Subject Matter

Claims 1 – 5, 7 – 10, 13 – 15 and 17 are allowed.

The following is a statement of reasons for the indication of allowable subject matter:

Re independent claims 1, 3, 7 and 13, the prior art of record does not teach or suggests in combination: "*using the clock adjustment hardware to adjust the local clock frequency until a threshold condition occurs; and after the threshold condition occurs, using the software program executing on the processing unit to adjust the local clock frequency, wherein the adjusting the frequency at which the local clock oscillates includes switching between using said clock adjustment hardware and using said clock adjustment software program executing on the processing unit to adjust the frequency at which the local clock oscillates.*".

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ARISTOCRATIS FOTAKIS whose telephone number is (571)270-1206. The examiner can normally be reached on Monday - Friday 7 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sam K. Ahn can be reached on (571) 272-3044. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Aristocratis Fotakis/

Primary Examiner, Art Unit 2611